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# Suppression of Short-channel Effects by Double-gate Double-channel Device Design in Normally-off AlGaIn/GaN MIS-HEMTs

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## ABSTRACT

In this work, we have performed numerical simulations of normally-off AlGaIn/GaN recessed Metal-Insulator-Semiconductor or MIS-HEMTs. A double-gate double-channel device design is proposed and analyzed using calibrated TCAD models. The dual-gate geometry is shown to provide an enhanced gate control over the double-channel, thereby suppressing the short-channel effects. The proposed device exhibits 72-mV/decade subthreshold slope, which is 50% improvement compared to the single-gate single-channel device with 3  $\mu\text{m}$  gate length. Both the double-gate double-channel and single-gate single-channel structures are compared for their ability to counter short-channel effects in aggressively scaled MIS-HEMT devices. It is shown that, double-gate design is superior to single-gate single-channel device with 80% improvement in drain-induced barrier lowering at sub-micrometer gate lengths.

## KEYWORDS

AlGaIn/GaN; double-channel; double-gate; MIS-HEMT; short-channel effects; subthreshold slope

## 1. INTRODUCTION

Wide bandgap GaN-based devices have been widely recognized as the future of high power and RF applications [1–3]. The reason for this growing acceptance of AlGaIn/GaN heterostructure as an alternative to Silicon-based power devices is attributed to the excellent material properties of III-Nitride semiconductors. In particular, the polarization-induced high-density high-mobility sheet-type charge region, also known as 2-D electron gas (2-DEG) at the heterointerface allows carrier transport with least scattering and loses thus, making AlGaIn/GaN devices suitable for power electronics [4,5].

Due to the presence of 2-DEG under the gate even in zero bias condition, AlGaIn/GaN high-electron-mobility transistor (HEMT) shows normally-on operation. However, it is a major roadblock in designing of fail-safe power switches, RF power amplifiers and simplified driving circuits in power electronics applications. As a solution, different architectures and techniques have been pursued for the design of normally-off enhancement mode devices with positive threshold voltages. These include metal-insulator-semiconductor (MIS) recessed gate, fluoride-based plasma treatment and AlGaIn back barrier layer structure etc. [6–9]. Further, recent advances for higher frequency operation of these devices have driven the gate length ( $L_g$ ) scaling down to the technological limit. Exceptionally high

cut-off frequency values of 562 GHz for 25 nm  $L_g$  and 547 GHz for 30 nm  $L_g$  In<sub>0.7</sub>Ga<sub>0.3</sub>As-In<sub>0.52</sub>Al<sub>0.48</sub>As HEMTs have been reported [10,11]. However, as  $L_g$  gets smaller, the device aspect ratio deteriorates and the appearance of short-channel effects (SCEs) overpowers the frequency response improvement, thus, limiting the continuous scaling in HEMTs. Hence, the device cannot be scaled unless the device aspect ratio is maintained by reducing vertical dimension which may result in increased gate leakage and loss of mobility.

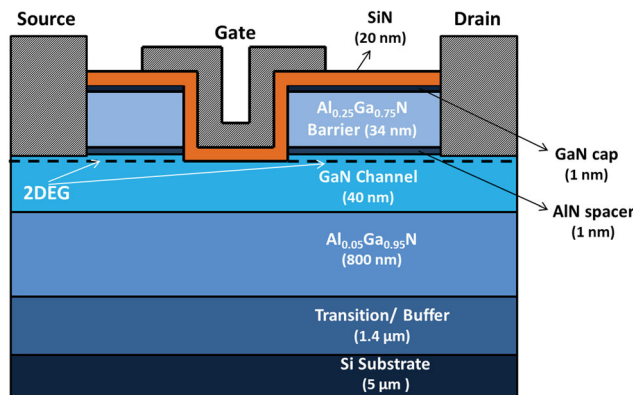
In order to continue with the RF performance enhancement without aggregating SCEs, alternate solutions involving structural modifications in the existing HEMT devices have been explored [10–12]. In this work, the concept of efficient charge control in double-gate geometry due to the presence of two gates along the channel has been utilized, where for the first time to our knowledge; we have reported a double-gate double-channel (DG-DC) device design for AlGaIn/GaN recessed MIS-HEMTs showing improved performance against SCEs when compared to its conventional counterparts.

Thorough physics-based investigation using commercial TCAD tools extensively aids in computational modeling of complex device architectures and related phenomena prior to real fabrication [13–17]. Thus, we too have used TCAD data for early exploration of the proposed

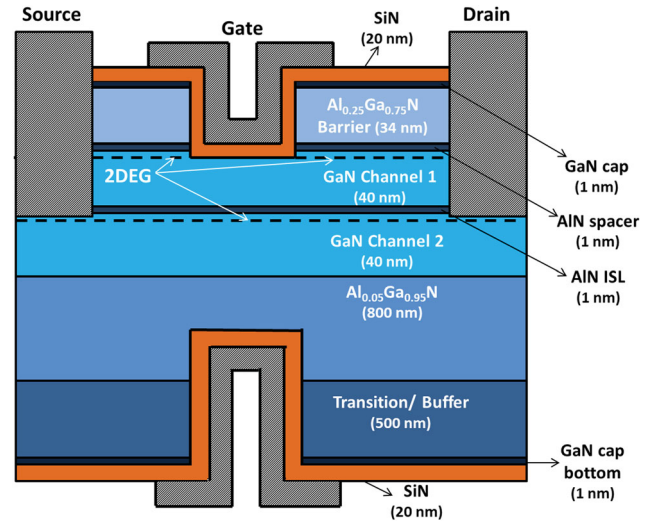
design. We first validated the TCAD models against the experimental data of single-gate single-channel (SG-SC) MIS-HEMT structure [6]. The calibrated deck is then used for investigating the performance of the proposed DG-DC architecture against the SCEs with respect to SG-SC MIS-HEMT. The organization of the paper is as follows: in Section II we present the details of the studied HEMT device and discuss the major TCAD device models and their impact on device operation. In Section III, we elucidate the proposed device structure and compare its performance with the standard SG-SC MIS-HEMT. Finally, the conclusion is presented in Section IV.

## 2. TCAD SETUP AND CALIBRATION

Figures 1 and 2 show the schematic of the normally-off SG-SC and proposed DG-DC AlGaIn/GaN recessed MIS-HEMT structure respectively. The nominal thickness and composition of all the layers are kept same as the fabricated device [6]. The simulated SG-SC structure comprises of an epitaxial stack grown over a Silicon substrate with AlN nucleation layer and  $\text{Al}_x\text{Ga}_{1-x}\text{N}$  transition layers, where Al composition is graded from 75% to 25% along with an additional 800 nm thick  $\text{Al}_{0.05}\text{Ga}_{0.95}\text{N}$  buffer layer. The transition layers act as a buffer to relax the strain due to lattice mismatch between the GaN channel and the substrate. This is followed by a 40 nm thick GaN channel which is separated from the 34 nm AlGaIn barrier by a 1 nm thick AlN layer. The barrier layer is covered by a 1 nm thick cap-layer of GaN. The gate region is then recessed such that cap and barrier layers are removed up to a certain depth within the GaN channel. Finally, a 20 nm thick SiN layer is placed over the capping layer which serves the dual purpose of device passivation and gate insulator.



**Figure 1:** Schematic cross-sectional view of the simulated SG-SC AlGaIn/GaN recessed MIS-HEMT structure



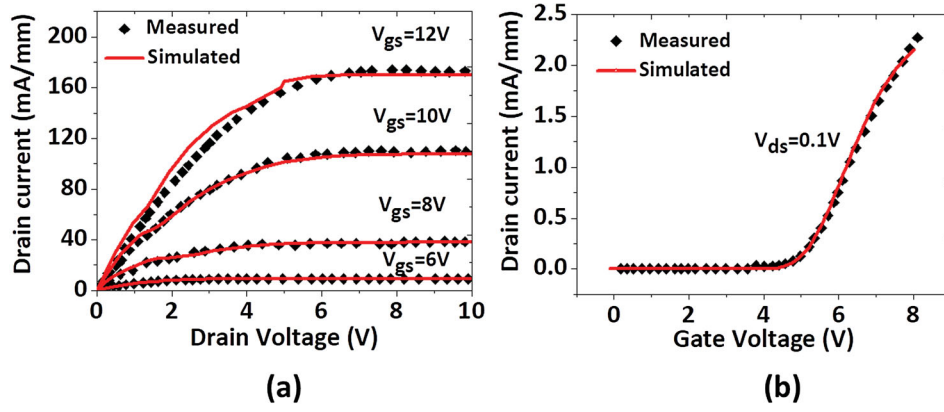
**Figure 2:** Schematic cross-sectional view of the proposed DG-DC AlGaIn/GaN recessed MIS-HEMT structure

The source and the drain regions are defined as ohmic contacts with resistance value  $1.8 \Omega\text{-mm}$  and W-based metal is utilized as the gate electrode. The lateral device dimensions include  $L_g = 3 \mu\text{m}$ , source-gate extension  $L_{sg} = 4 \mu\text{m}$  and gate-drain extension  $L_{gd} = 6.5 \mu\text{m}$ . Additionally, in order to obtain the same current density as the experimental data, realistic concentrations of fixed charges, donor and acceptor-traps are introduced in accordance with the data reported in the literature [13,14,16,18]. TCAD models that were validated in our previous work for the conventional Schottky-gate HEMT are now calibrated for the device described above [19,20]. Figure 3 shows the simulated  $I_{ds}-V_{ds}$  and  $I_{ds}-V_{gs}$  characteristics of the device, which are in good agreement with the published experimental data [6].

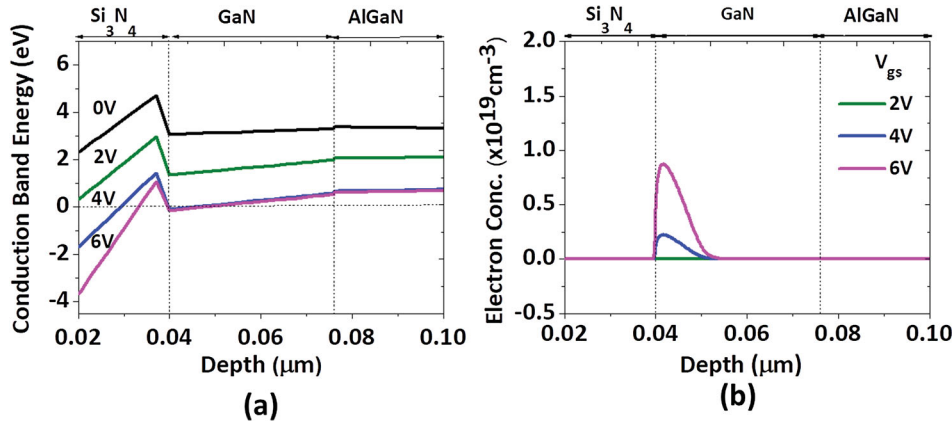
Very high sheet carrier concentrations of the order of  $10^{13} \text{ cm}^{-2}$  or more resulting from polarization-induced electric fields are obtained at hetero-junctions between different group III-Nitride materials even without intentional doping [1]. The total polarization along the epitaxial stack includes the spontaneous polarization and piezoelectric (strain-induced) polarization. In TCAD, the polarization-induced charges  $q_p$  are computed as discontinuity of polarization vector  $P$  at different material interfaces, which are then added to overall charge for determining the electrostatics of the device using the Poisson's equation [20,21].

$$q_p = A \cdot \nabla P \quad (1)$$

where,  $A$  refers to the activation constant, which is an important non-negative fitting parameter for computational modeling. In this work, we have taken



**Figure 3:** Measured and simulated (a)  $I_{ds}$ - $V_{ds}$  curve and (b)  $I_{ds}$ - $V_{gs}$  curve for SG-SC MIS-HEMT device. The simulated data correlates well with the experimental data from [6]



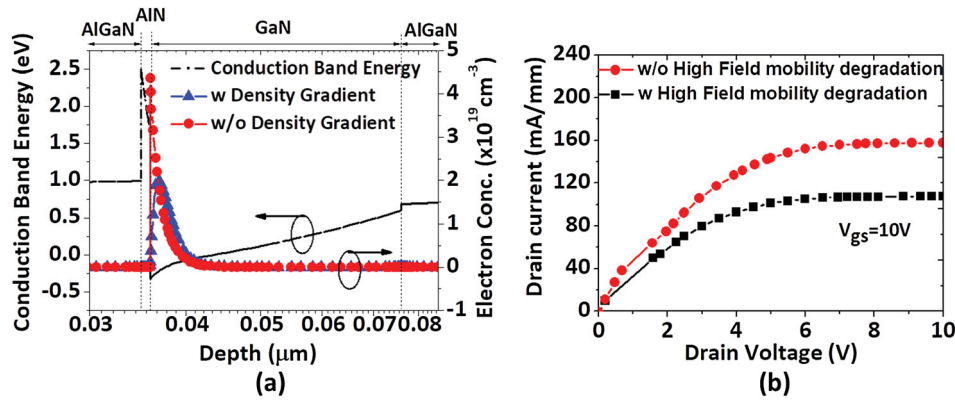
**Figure 4:** Effect of polarization and surface states on (a) Energy band profile and (b) Electron density for SG-SC HEMT as a function of  $V_{gs}$ . The cutline is along the middle of the gate electrode for  $L_g = 3 \mu m$

$A = 0.9$  for 2-DEG formed at the AlN/GaN heterointerface.

The surface states indicating surface defects, dangling bonds, and absorbed ions are experimentally known to exist at the dielectric/semiconductor interface despite the dielectric passivation [4]. If electrons transfer from donor-like surface states into empty lower energy states in GaN, it results in the formation of a positive surface charge sheet with negative charges in the channel. To model this effect we have included donor-like surface states of the order  $1 \times 10^{14} \text{ cm}^{-2}$  at an energy level of  $E_c - 0.6 \text{ eV}$  in our simulation setup. Figure 4(a) shows the energy band profile under the influence of polarization charges and gate bias ( $V_{gs}$ ). As the gate region is recessed through the cap and barrier layers, the continuous 2-DEG channel is interrupted resulting in the positive threshold. In addition, the presence of GaN/Al<sub>0.05</sub>Ga<sub>0.95</sub>N heterointerface induces negative polarization charges below the gate region, which further shifts the threshold to the positive side. Figure 4(b) shows the increase in the electron density in the 2-DEG channel with the applied  $V_{gs}$ .

The formation and confinement of 2-DEG in a narrow quantum well gives rise to quantum confinement effects, such as energy band splitting and reduced density of states, impacting threshold voltage ( $V_T$ ) and ON current of the device [13]. Hence, to include the quantization effects, we have used the density gradient quantization model in our simulations. The results in Figure 5(a) show that quantum confinement effects lead to a reduction in peak 2-DEG density. Also, this is to emphasize that the peak is no more situated at the interface but has shifted away into the channel.

At lower electric fields, the effect of doping density, temperature and field strength on carrier mobility is captured using the Farahmand Modified Caughey-Thomas model [22,23]. Similar expression has been suggested by Arora *et al.* to account for the enhanced scattering rate at higher temperatures [24]. The slope of  $I_{ds}$ - $V_{gs}$  curve at doping concentrations comparable to reference doping density is controlled by the fitting parameter  $\alpha$ . The value of  $\alpha$  is taken as 0.1 in this work. Accordingly, the low field mobility suitable for drift-diffusion simulations is evaluated



**Figure 5:** Effect of (a) quantum confinement on electron density and (b) drain current degradation due to inter-valley scattering at high fields in SG-SC HEMT

with parameter values for GaN as in [22]. The values for minimum and maximum mobility are 100 and 1600 cm<sup>2</sup> V<sup>-1</sup> s<sup>-1</sup>, respectively, as in [25].

Figure 5(b) depicts drain current degradation at high fields attributed to the phenomena of inter valley scattering. Attainment of sufficiently high energy results in transfer of electrons to energetically higher valley with a greater effective mass thus, resulting in mobility reduction. This negative differential mobility observed at higher driving fields is modeled as in [22]. Finally, to account for the mobility reduction due to acoustic surface phonon scattering and surface roughness caused by the strong electric fields normal to the current, Lombardi model is utilized in our simulations [25,26]. The carrier mobility is subsequently calculated by combining the surface contributions and bulk mobility according to the Matthiessen's rule.

### 3. RESULTS AND DISCUSSION

#### 3.1 Double-gate Double-channel Device Description

We have shown the proposed enhancement-mode AlGaIn/GaN DG-DC MIS-HEMT in Figure 2. The device consists of two channels; an upper channel formed at the AlGaIn barrier/GaN heterointerface and a lower channel at 1 nm thick AlN insertion layer (ISL) and bottom GaN heterointerface. The presence of lower channel is attributed to the strong polarization field at the interface of AlN-ISL and bottom GaN buffer layer. Also it has been shown that the presence of AlN layer increases the product of charge density and mobility in the channel [14]. The layer thickness and composition are considered such that the structure remains comparable to the SG-SC counterpart. The top gate is recessed similarly till

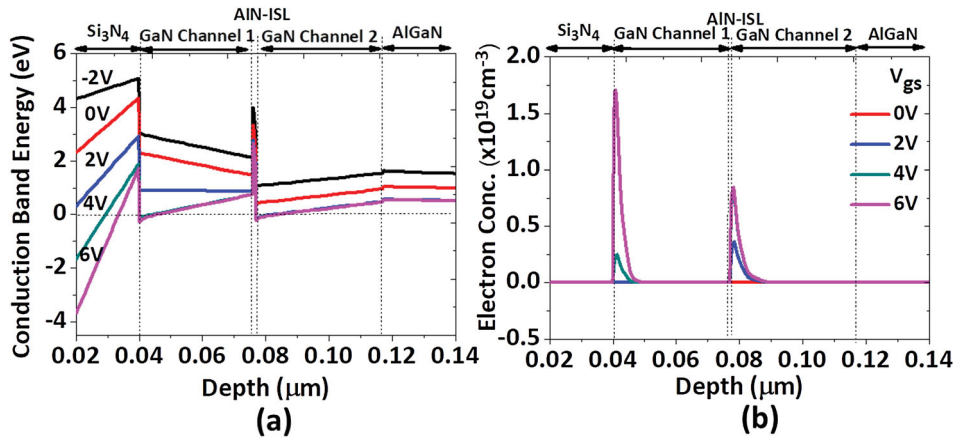
some part of the upper channel is removed thus pinching-off both the channels at zero  $V_{gs}$ . However, restricting the recess till upper channel reduces the surface roughness scattering as the lower channel is far away from the etched surface. In addition, a recessed bottom gate is introduced 300nm below the second GaN channel so as to increase the gate control efficiency of the device. The viability of such double-gate architectures has already been reported in recent studies where a symmetric AlInAs/InGaAs HEMT is designed with two gates placed on either side of the InGaAs channels using adhesive bonding technique [27].

The conduction band energy profile at the recessed gate region as a function of  $V_{gs}$  is shown in Figure 6(a). Both the channels are pinched-off at zero  $V_{gs}$  thus ensuring normally-off operation. The lower channel starts conducting at a lower  $V_{gs}$ , subsequently followed by the upper channel. The same is depicted in Figure 6(b) that shows the electron densities in the two channels increasing with  $V_{gs}$ . It is worth noting that as  $V_{gs}$  increases, electron density in the lower channel rises until the upper channel turns on. Thereafter, lower channel density saturates as it is screened from the gate control due to the formation of the upper channel.

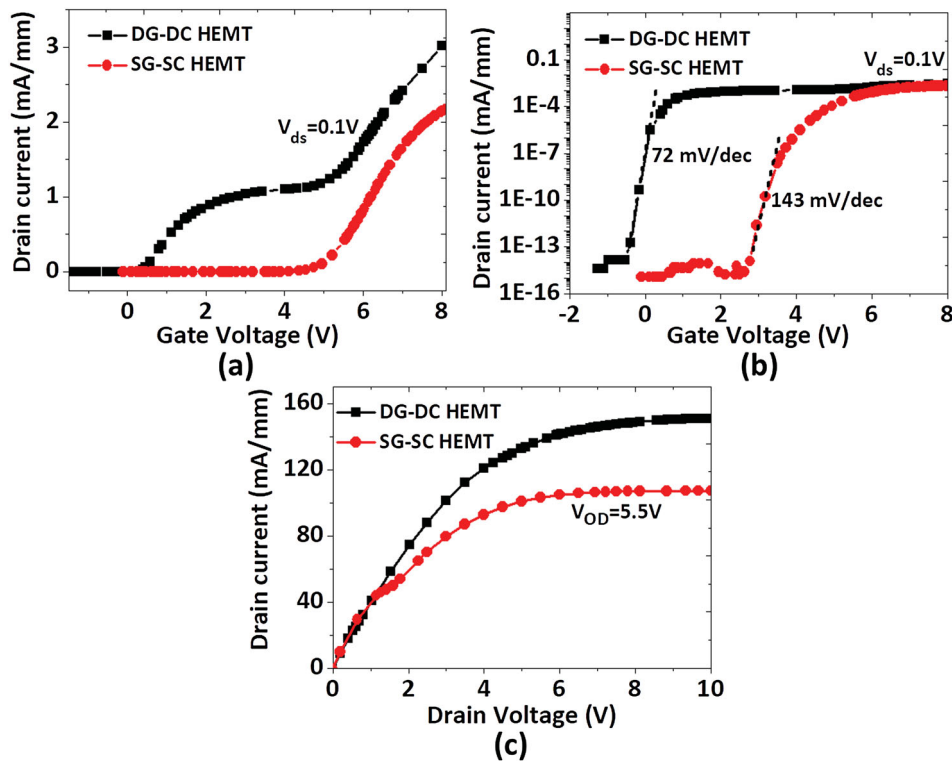
#### 3.2 Comparison Between DG-DC and SG-SC HEMTs

The simulated  $I_{ds}-V_{gs}$  characteristics of the DG-DC HEMT is compared with the SG-SC HEMT in Figure 7(a) for  $L_g = 3\mu\text{m}$ . Note that both the top and the bottom gate electrodes for the DG-DC device are at the same potential. It is observed from Figure 7(a) that the drain current in DG-DC device is 50% more than the SG-SC device owing to the presence of two 2-DEG channels. Also, a relatively flat segment is observed in the  $I_{ds}-V_{gs}$  curve





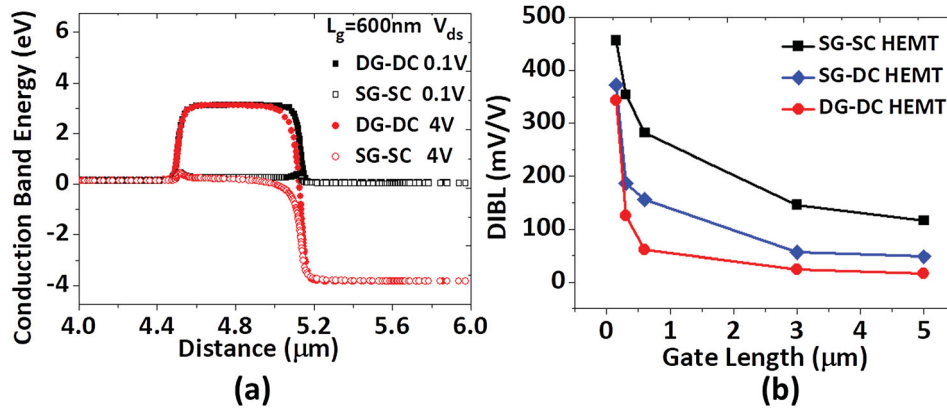
**Figure 6:** Effect of  $V_{gs}$  on (a) Energy band profile and (b) Electron density for DG-DC HEMT. The cutline is taken along the middle of the gate electrode for  $L_g = 3 \mu m$



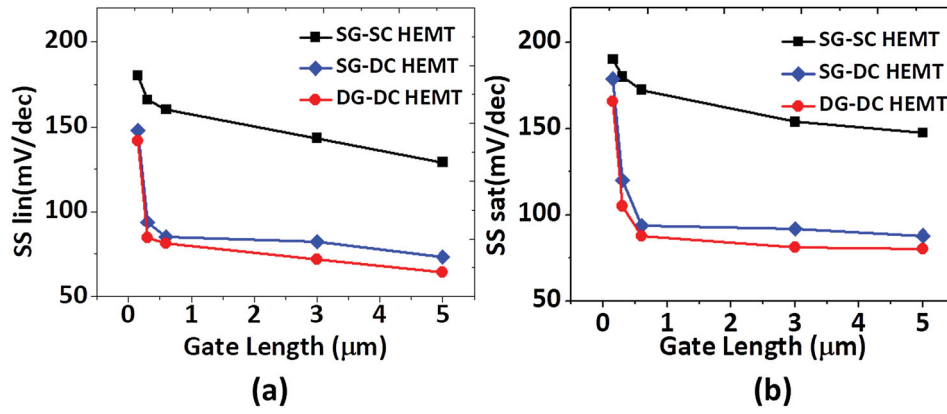
**Figure 7:** Comparison of DG-DC and SG-SC HEMT for  $L_g = 3 \mu m$ .  $I_{ds}$ - $V_{gs}$  characteristics on (a) linear scale (b) semi-log scale and (c)  $I_{ds}$ - $V_{ds}$  characteristics at  $V_{g,OD} = 5.5 V$

for  $V_{gs}$  varying from 2 to 4V approx. which indicates the prominent double-channel behavior of the device. As  $V_{gs}$  increases from 0 V, the lower channel is turned on and starts conducting first. With an increasing  $V_{gs}$ ,  $I_{ds}$  increases until the upper channel begins building up and lower channel is screened from the gate control. At this point, the transfer characteristic is hit by a plateau which indicates saturation of 2DEG in the lower channel and gradual turning on of upper channel (see Figure 6(b)). Once a continuous upper channel is formed, again a rise

in  $I_{ds}$  is observed with increasing  $V_{gs}$ . Figure 7(b) shows the transfer characteristics of both the devices plotted on a semi-log scale. Using constant current method [28],  $V_T$  of DG-DC device is found to be 0.462V. The subthreshold slope at  $V_{ds} = 0.1V$  (SS linear) of DG-DC HEMT is determined to be 72 mV/decade, which is 2 times better than SS linear of SG- SC HEMT (143 mV/decade). The  $I_{ds}$ - $V_{ds}$  curves in Figure 7(c) shows an improvement of over 40% in the drain current at a gate over-drive voltage  $V_{g,OD} = 5.5 V$ .



**Figure 8:** Comparison of (a) Energy band profiles along the channel at a gate under-drive voltage of  $-2$  V for  $L_g = 600$  nm device and (b) DIBL versus  $L_g$  for DG-DC, SG-DC and SG-SC HEMT



**Figure 9:** Comparison of (a) SS linear at  $V_{ds} = 0.1$  V and (b) SS saturation at  $V_{ds} = 4$  V versus  $L_g$  for DG-DC, SG-DC and SG-SC HEMT

In the smaller-geometry devices, the channel potential is influenced by both the  $V_{gs}$  and  $V_{ds}$ , making it increasingly susceptible to SCEs. The decrease in the potential barrier of the channel is observed with an increase in  $V_{ds}$  and is called as drain-induced barrier lowering (DIBL). The reduction of the potential barrier modifies  $V_T$ , eventually allowing electron flow between the source and the drain under the influence of the lateral electric field at  $V_{gs} < V_T$ . The channel current that flows under this conditions is called the sub-threshold current. Another significant effect observed in small-scale devices is an increase in SS with  $L_g$  scaling. Deterioration of the subthreshold behavior results in an increase in standby power dissipation due to rising off-current. In order to investigate the role of dual-gate architecture in DG-DC device for its efficacy in suppressing the SCEs,  $L_g$  is varied between  $5 \mu\text{m}$  to  $150$  nm. The 1-D conduction band energy profiles along the channel for  $L_g = 600$  nm device is shown in Figure 8(a) for a gate under-drive voltage of  $-2$  V. The  $V_{gs}$  is chosen such that both the devices are pinched-off in absence of DIBL. It is seen that improved channel confinement in DG-DC HEMT not only provides a greater potential barrier in pinch-off but also

suppresses the voltage shift due to DIBL under the same scaling condition. Figure 8(b) compares DIBL in DG-DC and SG-SC HEMT for different  $L_g$ , where DIBL is calculated as:

$$\frac{(V_{T,V_{ds}=4V} - V_{T,V_{ds}=0.1V})}{(4V - 0.1V)} \quad (2)$$

Improvement of 78% is seen in DIBL at  $L_g = 600$  nm in DG-DC HEMT as compared to SG-SC HEMT. Further, a single-gate double-channel device (SG-DC) is simulated and compared for DIBL performance. Results show that in absence of bottom gate, the electrostatic control over the channel potential degrades. However, the device still performs better over SG-SC geometry with 45% improvement in DIBL at  $L_g = 600$  nm.

Further, SS for the devices at linear and saturation drain bias are compared. SS is defined as the change in  $V_{gs}$  bringing about a decade change in  $I_{ds}$ . Mathematically, it is given as:

$$SS = \frac{\partial V_{gs}}{\partial \log I_{ds}} \quad (3)$$

As shown in Figure 9(a and b), SG-SC HEMT experiences a significant degradation of 26–31 mV/decade in SS as we scale from 5  $\mu\text{m}$  to 600 nm gate lengths at higher drain bias. On the other hand, DG-DC HEMT maintains a relatively constant SS under the same scaling conditions owing to better gate control. Again, DG-DC HEMT outperforms the SG-SC HEMT at  $L_g = 600$  nm and  $V_{ds} = 4$  V with SS  $\sim 88$  mV/decade against 172 mV/decade for SG-SC HEMT. The SG-DC device shows an intermediate performance with SS  $\sim 94$  mV/decade.

#### 4. CONCLUSION

A TCAD-based high-performance DG-DC enhancement mode AlGaIn/GaN recessed gate MIS-HEMT device design has been proposed. TCAD model calibration is performed by comparing the simulation results for a standard SG-SC MIS-HEMT against the published experimental data. These calibrated TCAD models are then utilized for the analysis of the proposed DG-DC devices. DG-DC HEMTs show an enhanced drain current and improved subthreshold slope as compared to the SG-SC devices. Simulations at different  $L_g$  reveal robustness of the DG-DC HEMTs in countering short-channel effects. At sub-micrometer gate lengths with almost 80% DIBL and 50% subthreshold slope improvement over SG-SC devices, DG-DC HEMTs are promising for high-performance scaled applications.




#### DISCLOSURE STATEMENT

No potential conflict of interest was reported by the authors.

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