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Toward novel designs of reversible ternary 6:2 Compressor using efficient reversible ternary full-adders

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Abstract

Integrated circuits always face with two major challenges including heat caused by energy losses and the area occupied. In recent years, different strategies have been presented to reduce these two major challenges. The implementations of circuits in a reversible manner as well as the use of multiple-valued logic are among the most successful strategies. Reversible circuits reduce energy loss and ultimately eliminate the problem of overheating in circuits. Preferring multiple-valued logic over binary logic can also greatly reduce area occupied of circuits. When switching from binary logic to multiple-valued logic, the dominant thought in binary logic is the basis of designing computational circuits in multiple-valued logic, and disregards the capabilities of multiple-valued logic. This can cause a minimal use of multiple-valued logic capabilities, increase complexity and delay in the multiple-valued computational circuits. In this paper, we first introduce an efficient reversible ternary half-adder. Afterward, using the reversible ternary half-adder, we introduce two reversible versions of traditional and comprehensive reversible ternary full-adders. Finally, using the introduced reversible ternary full-adders, we propose two novel designs of reversible ternary 6:2 Compressor. The results of the comparisons show that although the proposed circuits are similar to or better than previous corresponding designs in terms of criteria number of constant input and number of garbage outputs, they are superior in criterion quantum cost.

Keywords Reversible logic · Ternary logic · Half-adder · Full-adder · Compressor

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1 Introduction

Occupied area and energy dissipation are considered as two challenging issues in VLSI industry. One of the solutions presented to reduce the occupied area, increasing speed and decreasing circuit complexity, is the use of multiple-valued logic (MVL) in circuit design. Ternary logic is one of the most popular multiple-valued logic that has attracted researchers in recent years [1]. Another issue that is very important in the design of integrated circuits which is increasingly getting significant is the issue of power consumption and energy losses reduction otherwise the smallest loss of energy in VLSI circuits causes too much heat and thus reduces the life and efficiency of the circuits. A solution that has attracted the attention of many digital designers in recent years is reversible circuits. Bennett has proven that circuit design in reversible form can remove the energy losses caused by missing information in the circuit [2]. A circuit is reversible if the number of inputs is equal the number of outputs and there is a one-to-one correspondence between inputs and outputs [3].

Due to the prominent features of reversible ternary circuits, so far many circuits including adders and subtractors [4–8], comparators [9], multipliers [10, 11] as well as various base circuits [12–16] have been designed and implemented.

Compressor is a digital modern circuit that is applied for high speed with minimum gates. Compressors are designed using full-adder, which is an essential component of many computational systems.

So far, several reversible ternary full-adders have been designed which will be discussed in more details in Sect. 3.

One of the major problems of all previous designs is the absence of full use of the capacity of the full-adder. Basically, a full-adder at the radix of r is capable of receiving $(r+1)$ inputs and produce two outputs with different values. So, we have used this potential and presented a comprehensive reversible ternary full-adder. The most prominent feature of the introduced reversible ternary full-adder compared to all previous traditional reversible ternary full-adders is that it does not produce an additional digit in consecutive additions and so can perform computations with the least circuit complexity and fastest speed compared to existing traditional ternary full-adders.

The highlights of this paper are summarized as follows:

- Introducing an efficient reversible ternary half-adder
- Introducing a traditional reversible ternary full-adder using the reversible ternary half-adder
- Introducing a comprehensive reversible ternary full-adder by inspiring ternary potential
- Proposing two novel designs of reversible ternary 6:2 Compressor using the introduced full-adders

The paper is composed of the following sections: an overview of ternary logic, reversible logic and reversible ternary circuits are given in Sect. 2. In Sect. 3, we

will review the previous reversible ternary full-adders. The proposed reversible ternary 6:2 Compressor circuits are provided in Sect. 4. The comparisons are presented in Sect. 5. Finally, the paper finalizes with conclusions and future works.

2 Foundations of the research

In order to have a better understanding of reversible ternary Compressor circuit design, this section briefly discusses the basics of the work. The most important basic topics in this article are reversible logic, ternary logic and basic reversible ternary gates.

2.1 Ternary logic

It is predicted that in recent years we will reach a fundamental limit for heat dissipation from integrated circuits. One way to reduce the complexity of circuits to some extent and thus reduce energy wastage in different technologies is to use multiple-valued logic. Among the multiple-valued logic, ternary logic has been considered by many researchers today [16–22]. Since the circuits designed in this article are all ternary, we will have a very brief overview of this logic in this section.

In this logic, three values of 0, 1 and 2 are used. To design different circuits in this logic, five main operations are considered, which can be applied to their inputs in both conditional and unconditional modes [17, 23]. These actions are summarized below:

1. Add a unit to the input. This operation is indicated by the symbol "+ 1". Obviously, if the calculated value is more than two, the remainder is calculated to be 3 and is shown in the output. Figure 1 shows an overview of this operation.
2. Add two units to the input. This operation is indicated by the symbol "+ 2". Obviously, if the calculated value is more than two, the remainder is calculated to be 3 and is displayed in the output. Figure 2 shows an overview of this operation.
3. Replace the "zero" and "one" input values. This operation is indicated by the symbol "01". That is, if the input was "zero", it would become "one" after this operation, and if the input was "one", it would become "zero" after this operation. Obviously, if the input was "two", it would not change after this operation. Figure 3 shows an overview of this operation.

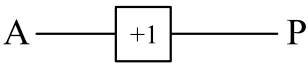


Fig. 1 Reversible ternary "+ 1" operation

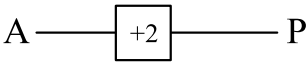


Fig. 2 Reversible ternary "+ 2" operation

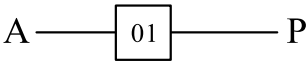


Fig. 3 Reversible ternary "01" operation

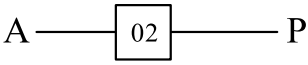


Fig. 4 Reversible ternary "02" operation

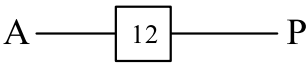


Fig. 5 Reversible ternary "12" operation

4. Replace the values of "zero" and "two" inputs. This operation is indicated by the symbol "02". That is, if the input was "zero", it would become "two" after this operation, and if the input was "two", it would become "zero" after this operation. Obviously, if the input was "one", it would not change after this operation. Figure 4 shows an overview of this operation.
5. Replace the "one" and "two" input values. This operation is indicated by the symbol "12". That is, if the input was "one", it becomes "two" after this operation, and if the input was "two", it becomes "one" after this operation. Obviously, if the input is "zero", it will not change after this operation. Figure 5 shows an overview of this operation.

As mentioned earlier, these operations can be applied unconditionally to any circuit input, or they can have a condition base and be applied by checking that condition base. Either way, each of these operations has a quantum cost of one.

2.2 Reversible logic

Another way to reduce wasted energy that can reduce heat generated independent of manufacturing technology to zero is to reversibly design the circuits [24–27]. In designing such circuits, three principles must be considered. The first and most important principle is that the inputs and outputs are one by one. This principle means that in addition to the number of inputs and outputs must be equal, there must be a specific output for each specific input. The second principle is the lack of feedback in the designed circuits, and finally the third principle is the absence of branching in any part of the circuit [28]. If we follow these three principles in the design, we will have a reversible circuit in which the energy loss due to the miss of information will be zero. It should also be noted that if the circuit is designed to consist of different gates and modules, all of these gates and modules must be reversible.

The next point in reversible circuits is the synthesis of such circuits, which is very different from the synthesis of traditional non-reversible circuits. In short, to design an efficient reversible circuit, the following points should be considered [29]:

1. The designed circuit must have the lowest quantum cost. Quantum cost is the number of 1×1 or 2×2 gates used to build reversible and quantum circuits. It should be noted that the quantum cost of 1×1 or 2×2 gates is considered one.
2. The output that is not used in later steps is called garbage or ancila. Since this information is unused and was created only to make the circuit reversible, it should be tried to design the circuit so that these outputs are minimized.

3. The circuit should be designed so that it has the least constant input. A constant input is an input that always has a constant value and is created only to make the circuit reversible.

2.3 Quantum reversible ternary gates

There are basic gates for the logical design of circuits with any logic and technology, with which the rest of the circuits are usually designed and implemented. Since the base gates of binary circuits, namely And, Or, etc., are not reversible and cannot be used in quantum circuits, so researchers have designed different gates to design reversible ternary circuits, the most important of which are as follows:

1. Reversible ternary gate NOT: This reversible gate has one input and one output. The figure and its truth table can be seen in Fig. 6 and Table 1.
2. Reversible ternary gate M-S: This reversible ternary gate has two inputs and two outputs, the first input is copied directly to the output and if the value of the first input is "two", the operation on the second input applies, otherwise the second input is copied directly to the output. Because one of the inputs is copied exactly to the output, this gate is called a one-through gate. Figure 7 shows an overview of this gate.
3. Feynman reversible ternary gate family: In general, a Feynman gate can be defined with k inputs and k outputs, but Feynman gate with two inputs and two outputs is one of the most important reversible ternary gates, and in technology various applications such as quantum technology have been implemented. According to Fig. 8, there are two types of Feynman gates, include normal Feynman gate and controlled Feynman gate.
1. Toffoli reversible ternary gate: Toffoli gate with k-input has k-1 inputs for control, which are copied directly to the output. The operation is performed on the last input, if all control inputs are two, otherwise, the last input is copied directly to

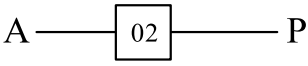


Fig. 6 Reversible ternary NOT gate

Table 1 Ternary NOT truth table

Input	Output
0	2
1	1
2	0

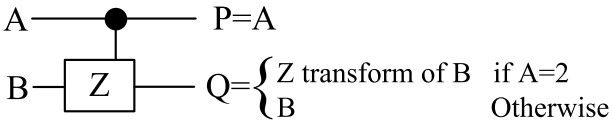


Fig. 7 M-S gate

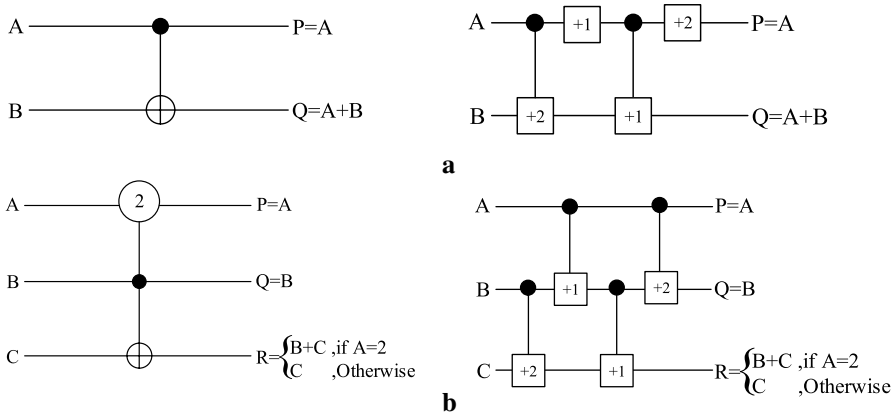


Fig. 8 Different representations of the quantum reversible ternary Feynman gate and its implementation using the M-S gate. **a** Normal mode and **b** controlled mode [30]

the last output. Because k-1 inputs are copied directly to the output, a k-input Toffoli gate is a k-1-through gate. For example, a three-input Toffoli gate is a two-through gate. Figure 9 shows an overview of 3-input of this gate.

2. Generalized quantum ternary gate (GTG): This reversible ternary gate has two inputs and two outputs, the first input is copied directly to the output and if the value of the first input is "zero", "one or "two", the operation on the second input applies. Because one of the inputs is copied exactly to the output, this gate is called a one-through gate [32]. Figure 10 shows an overview of this gate.

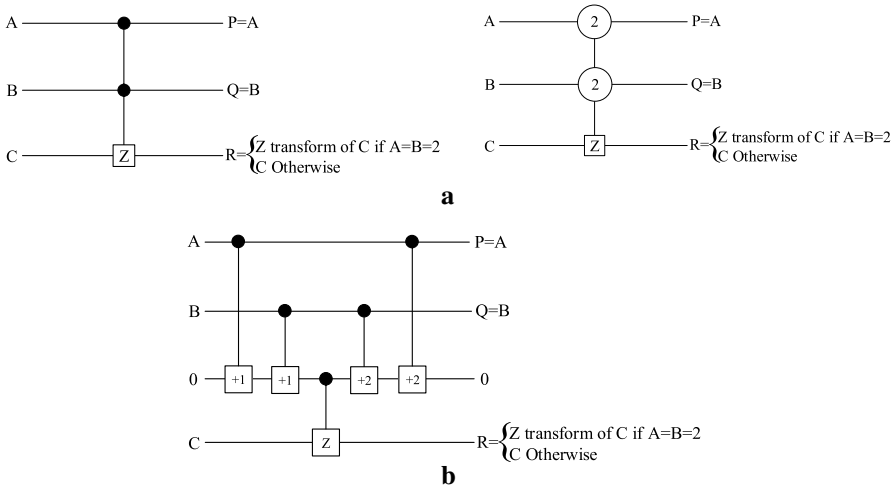


Fig. 9 Normal quantum reversible ternary Toffoli gate, **a** two different symbols and **b** realization using M-S gate [31]

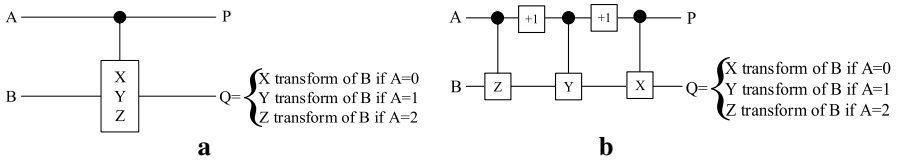


Fig. 10 GTG quantum reversible ternary gate, **a** circuit structure and **b** its implementation using M-S gate [32]

3 Overview of the previous quantum reversible ternary full-adders

Since the design of a reversible ternary Compressor has not been presented yet for consideration in this article, so this section provides a very brief overview of the most important part of a Compressor, namely the reversible ternary full-adder. In this section will provide a comprehensive overview of all the previous quantum reversible ternary full-adders.

The first quantum reversible ternary full-adder circuit was introduced in 2004 by Khan et al. [32]. The quantum realization of this full-adder is shown in Fig. 11. This design consists of ten GTG gates. Since the GTG gate has a quantum cost of 5, so the quantum cost of this full-adder is 50.

In the same year, Miller et al. developed another design for a reversible ternary full-adder circuit. How to implement this quantum ternary circuit can be seen in Fig. 12. The final quantum cost for the design presented by Miller et al. Is 102.

Three years later, a new circuit resulting from two half-adders was introduced by Khan et al. As shown in Fig. 13, this circuit is made up from two half-adders. The quantum cost per each half-adder in the presented circuit by Khan et al. was 25. Therefore, the total quantum cost of their presented circuit was 50.

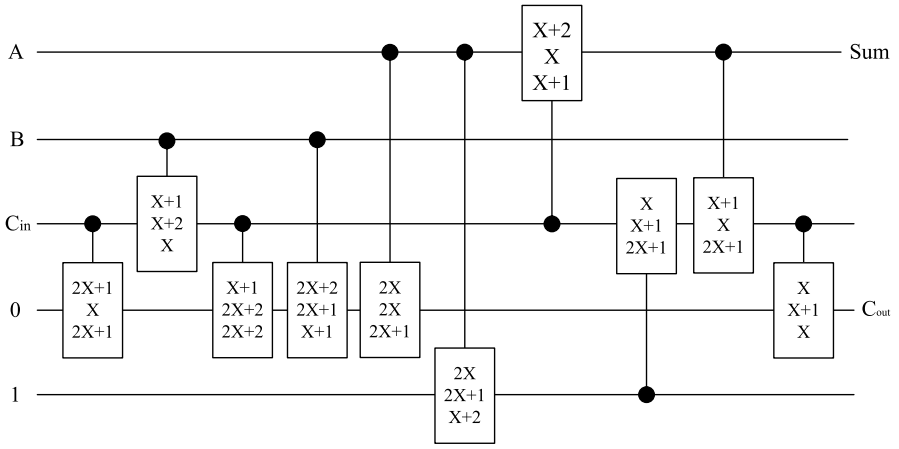


Fig. 11 The quantum representation of the quantum reversible ternary full-adder provided by Khan et al. [32]

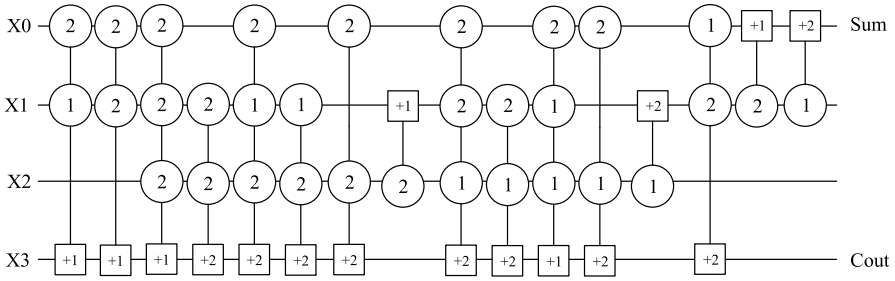


Fig. 12 Quantum representation of the quantum reversible ternary full-adder presented by Miller et al. [31]

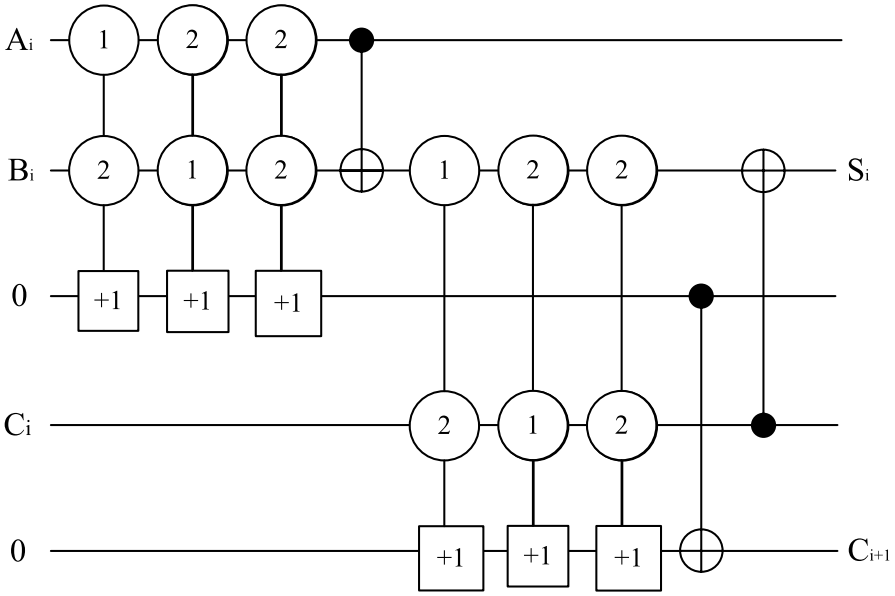


Fig. 13 Quantum representation of the quantum reversible ternary full-adder presented by Khan et al. [6]

In 2011, Mandal et al. implemented a new plan to reduce the quantum cost of reversible ternary full-adders. In this plan, they reduced the quantum cost to 42. The quantum circuit implemented by them can be seen in Fig. 14.

In 2015, Deibuk et al. used a genetic algorithm to investigate different scenarios for implementing a reversible ternary full-adder circuit. The result was a significant reduction in quantum cost and circuit size. They were able to reduce the quantum cost of a reversible ternary full-adder circuit to 14. An overview of their given circuit can be seen in Fig. 15.

In the same year, Lisa et al. designed a circuit with a quantum cost of 26. As shown in Fig. 16, their design is also symmetrical and consists of two half-adders.

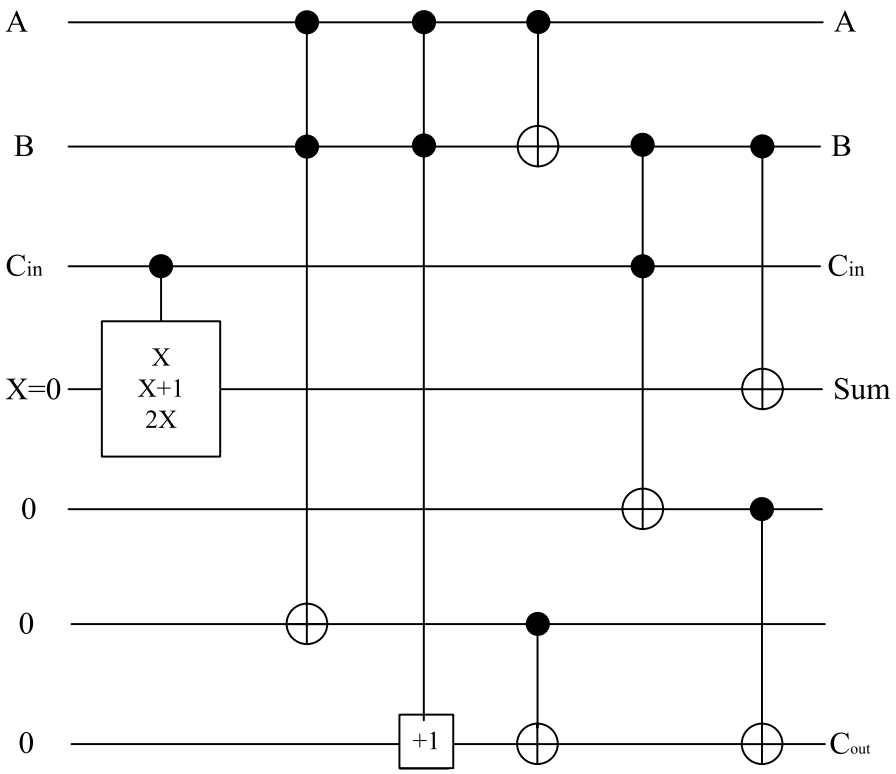


Fig. 14 Quantum representation of the quantum reversible ternary full-adder presented by Mandal et al

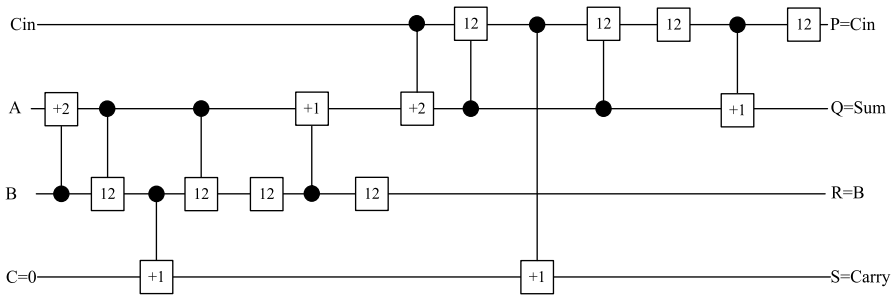


Fig. 15 Quantum representation of the quantum reversible ternary full-adder presented by Deibuk et al. [8]

In 2016, Haghparast et al. designed a circuit with a quantum cost of 34. As shown in Fig. 17, their design is also symmetrical and consists of two half-adders.

In the same year, Khan et al. developed a new method for synthesizing and designing reversible ternary circuits. Using their suggested method, they implemented a reversible ternary full-adder circuit. The result was a very large size circuit

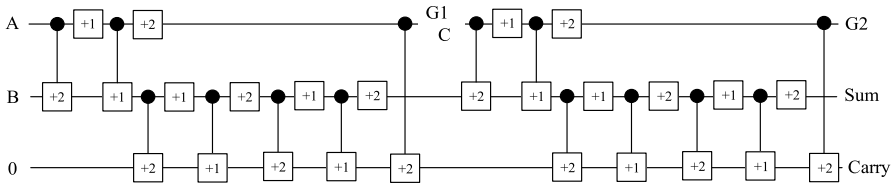


Fig. 16 Quantum representation of the quantum reversible ternary full-adder presented by Lisa et al. [7]

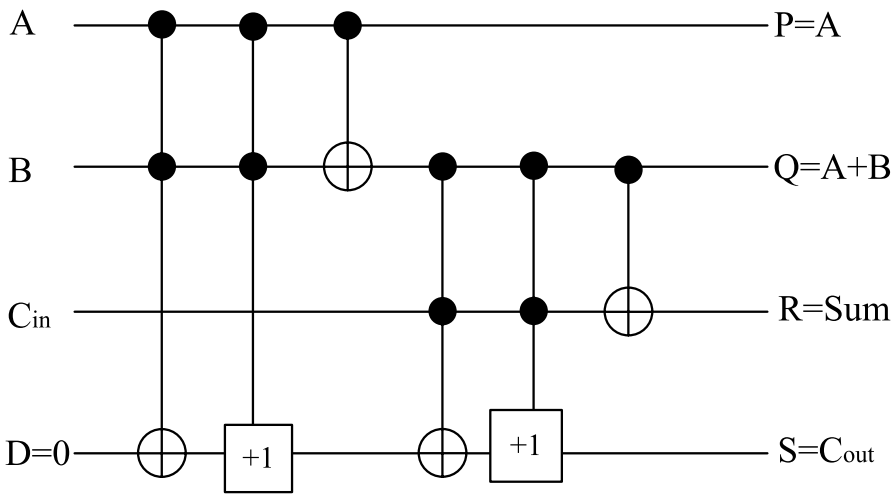


Fig. 17 Quantum representation of the quantum reversible ternary full-adder presented by Haghparast et al. [33]

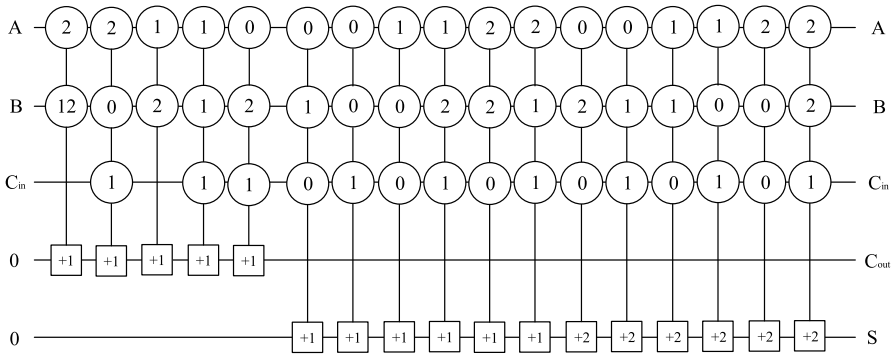


Fig. 18 Quantum representation of the quantum ternary-reversible full-adder presented by Khan et al. [34]

and very high quantum cost. The quantum cost of the circuit was 181. Their design is shown in Fig. 18.

In 2017, Haghparast et al. presented a circuit with minor changes to the circuit of Deibuk et al. You can see their circuit, which has a quantum cost of 14, in Fig. 19.

4 Proposed reversible ternary 6:2 Compressor

The performance of many modern computing systems is based on binary logic. When we migrate from binary logic to multiple-valued logic, it is observed that prevailing think in the design of computational circuits in multiple-valued logic is also based on binary logic, and potential capabilities of this logic are totally disregarded. This can increase the complexity and delay of the computational circuits in multiple-valued logic.

4.1 Basics of this design

In order to clarify this issue, in particular, we investigate the structure of binary and ternary full-adder circuits. A binary full-adder is a circuit that is capable of receiving three binary inputs with same value and producing two binary outputs with different values. When we examine the structure of existing traditional ternary full-adder circuits, we will find that the prevailing thinking in the design of all these full-adders is also inspired by binary full-adders. That is, traditional ternary full-adders receive three digits (trit) with same value and result two different value trits with different values. As we know, the largest two-trit number equivalents of the number $(22)_3$. The sum of three two-trit numbers $(22)_3$ using traditional ternary full-adders is illustrated in Fig. 20a. As can be observed, the final result of the sum is a four-trit number, that the leftmost digit always being zero. Therefore, the use of these types of ternary full-adders in ternary computational circuits will increase the complexity and delay of the circuits.

With reflection on multiple-valued computations, we come to a potential capability that underpins the design of our comprehensive ternary full-adder. Essentially, a full-adder at the radix of r can receive $(r+1)$ digits with same value at

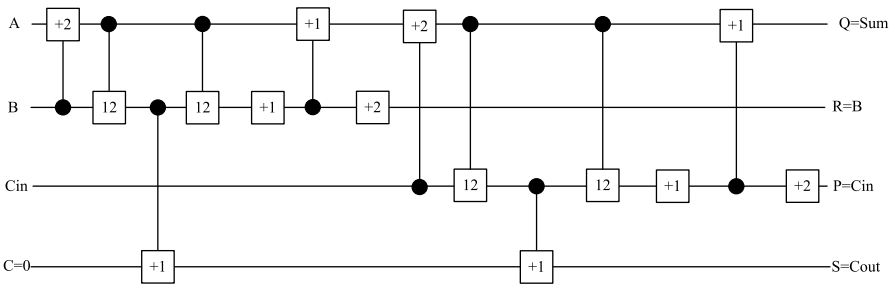


Fig. 19 Quantum representation of the quantum ternary-reversible full-adder presented by Haghparast et al. [35]

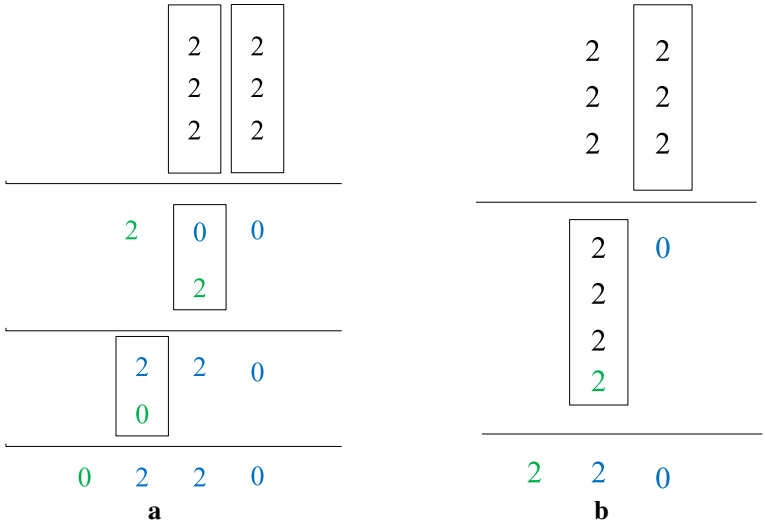


Fig. 20 An example of a sum of three two-trit numbers using **a** traditional ternary full-adders and **b** comprehensive ternary full-adder based on the introduced idea

the radix of r and result in two digits with different values at the radix of r. This is also easy to prove because the maximum value of each digit at the radix of r is $(r-1)$ and so the sum of $(r+1)$ numbers with value $(r-1)$ will be equal $[(r+1)\times(r-1)]=r^2-1$ that this value is the maximum value for a two-digit number at the radix of r. So, the sum of three two-trit numbers using comprehensive ternary full-adder based on the introduced idea is given in Fig. 20b.

As shown in Fig. 20, the use of the introduced ternary full-adder causes the sum of the results to be expressed by a three ternary digits and reduces the circuit delay too. Therefore, the use of the introduced ternary full-adder in consecutive summaries does not produce extra digits. This can reduce complexity and increase the speed of the circuit because the production of extra digit means the extra operation to produce a digit that its value is always zero.

4.2 Select the desired half-adder and full-adder

We proposed two traditional and comprehensive reversible ternary full-adders in [17] that its details are given in the following.

The introduced reversible ternary full-adders have been consisted of reversible ternary half-adders that its truth table is shown in Table 2.

As shown in Table 2, the carry digit occurs when one of the inputs is equal 2 and the other is greater than zero. The quantum realization of the introduced quantum reversible ternary half-adder along with its justifying for input vector (A, B) = (2,2) is shown in Fig. 21.

Table 2 Truth table of quantum reversible ternary half-adder

CI	*B*	*A*	Carry	Sum	*G*
0	0	0	0	0	1
0	0	1	0	1	1
0	0	2	0	2	1
0	1	0	0	1	2
0	1	1	0	2	2
0	1	2	1	0	2
0	2	0	0	2	0
0	2	1	1	0	0
0	2	2	1	1	0

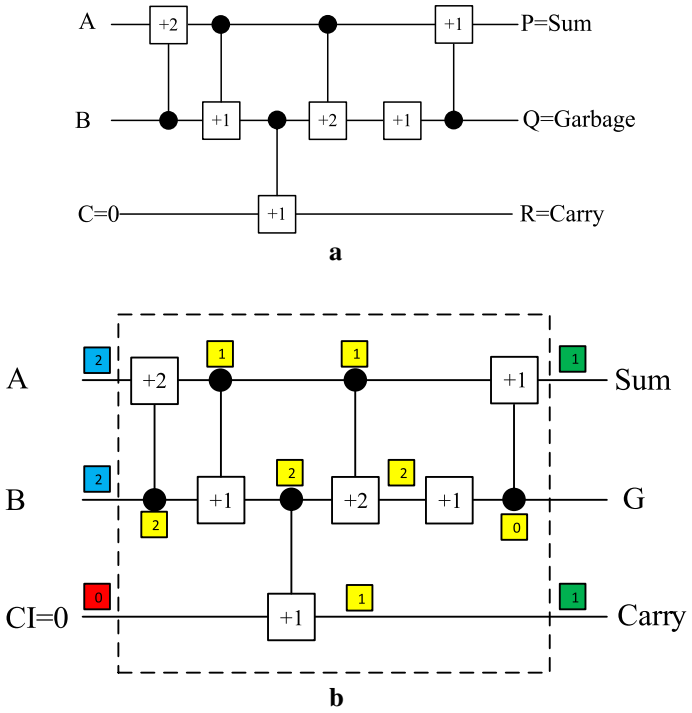


Fig. 21 The introduced reversible ternary half-adder **a** Quantum realization and **b** showing outputs for input vector (A, B) = (2, 2)

As shown in Fig. 21, in the quantum representation of the introduced quantum reversible ternary half-adder when the input CI is considered zero, the summation on the output P, the carry digit on the output R, and the garbage, whose value is B + 1, on the output Q are placed.

To implement the introduced quantum reversible ternary half-adder, a Shift gate and five M-S gates are used, with the quantum cost of each of these gates

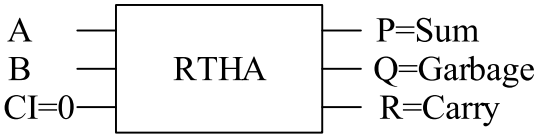


Fig. 22 Introduced quantum reversible ternary half-adder (RTHA) block diagram

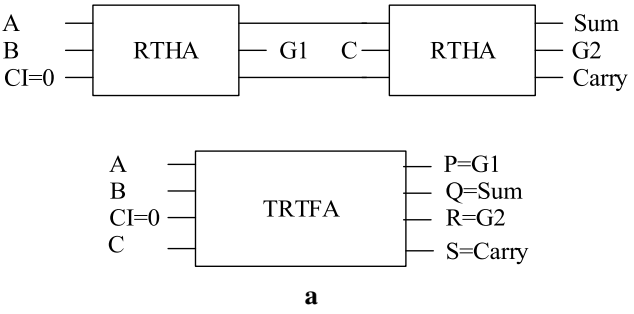


Fig. 23 Introduced quantum traditional reversible ternary full-adder (TRTFA) using two RTHA blocks **a** circuit representation, **b** quantum realization and **c** showing outputs for input vector (A, B, C) = (2, 1, 2)

being equal one. So, the quantum cost of the introduced quantum reversible ternary half-adder is 6. The introduced quantum reversible ternary half-adder (RTHA) block diagram is shown in Fig. 22.

The block diagram of the introduced quantum traditional reversible ternary full-adder (TRTFA) using the cascade connection of two RTHA blocks is shown in Fig. 23.

As shown in Fig. 23, since the introduced TRTFA circuit uses two RTHA blocks, its quantum cost is 12. Therefore, the TRTFA circuit has four inputs, including three main inputs and one constant input, as well as four outputs including two main outputs and two garbage outputs.

The block diagram of a quantum comprehensive reversible ternary full-adder (CRTFA) using the cascade connection of three RTHA blocks is shown in Fig. 24. As shown in Fig. 24, the circuit has five inputs including four main inputs (A, B, C, D) and one constant input as well as five outputs including two main outputs (Sum, Carry) and three garbage outputs (G1, G2, G3). Since the design of the quantum comprehensive reversible ternary full-adder (CRTFA) uses three RTHA blocks, it has a quantum cost of 18.

4.3 Proposed compressors

Multiplication is one of the main computation functions that can be widely used in digital systems. Multipliers are widely used in microprocessors, digital signal processing, image processing and many approximate computing applications. On the other hand, multipliers are usually on the critical path of these systems and

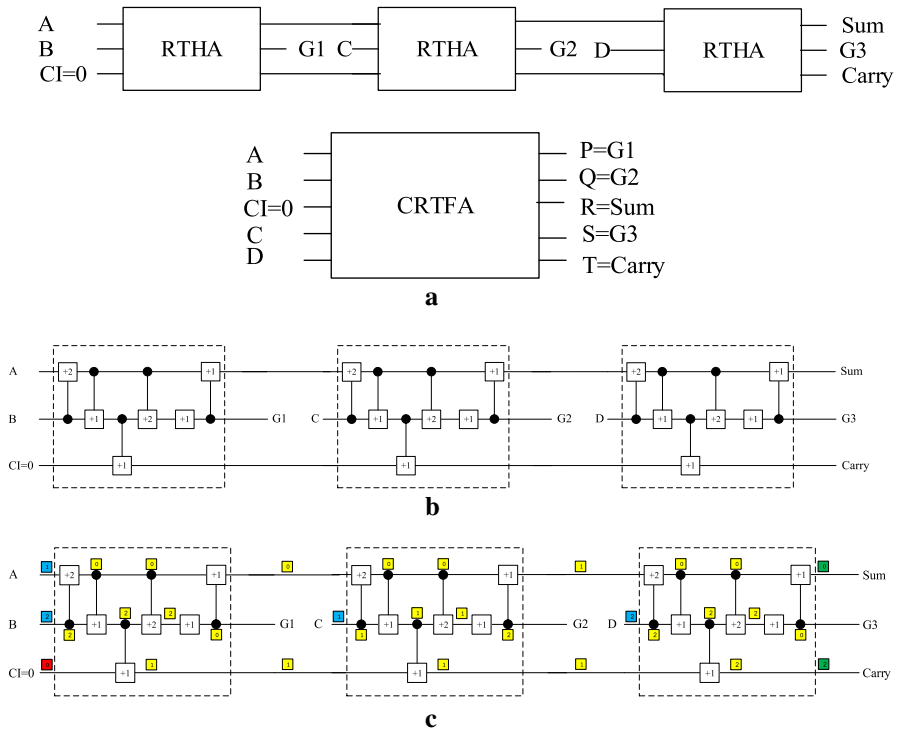


Fig. 24 Proposed quantum comprehensive reversible ternary full-adder (CRTFA) using three proposed RTHA blocks **a** circuit representation, **b** quantum realization and **c** showing outputs for input vector (A, B, C, D) = (1, 2, 1, 2)

significantly affect their propagation delay and power consumption. The parallel multiplication operation is carried out in three stages, including the production of partial products, reduction of the partial products to two rows and finally the sum of the two remaining rows [36]. Considering these three parts, the second part has a great impact on the design complexity, delay and power consumption. Therefore, increasing the efficiency of this step by using appropriate arithmetic blocks such as Compressors can directly improve the performance and efficiency of parallel multipliers. In fact, the use of Compressors can reduce energy loss by reducing the number of partial products in a multiplier. A Compressor k-m is a circuit with k inputs and m outputs whose total weight of its inputs equals to 2^i and weights of its main outputs are 2^i, 2^{i+1},… and 2^{i+m-1}. Compressors, in addition to the main inputs and outputs, have several inputs (weighing 2^i) from the previous neighbor blocks and several outputs (weighing 2^{i+1} or higher) to the next neighbor blocks.

A 6:2 Compressor is a circuit with nine inputs and five outputs that is shown in Fig. 25. As you can see, this Compressor has six main inputs x_1, x_2, x_3, x_4, x_5 and x_6 and three other inputs C_{in1}, C_{in2} and C_{in3} which receive their values from the previous neighbor Compressor. All nine inputs are same weight. Compressor 6:2 produces a Sum output of similar in weight to the inputs and four outputs of Carry, C_{out1}, C_{out2} and C_{out3} with one higher weight. The outputs of C_{out1}, C_{out2} and C_{out3} go to the next neighbor Compressor. All 6:2 Compressors with different designs follow Eq. 1:

$$X_1 + X_2 + X_3 + X_4 + X_5 + X_6 + C_{in1} + C_{in2} + C_{in3} = \text{Sum} + 2\left(\text{Carry} + C_{out1} + C_{out2} + C_{out3}\right) \tag{1}$$

Figures 26 and 27 show two new designs of a quantum reversible ternary 6:2 Compressor using the proposed TRTFA and CRTFA circuits. As shown in Fig. 25, since the first design requires four proposed TRTFA blocks, the quantum cost of this design equals 48, the number of constant inputs and the garbage outputs are 4 and 8, respectively. As we will see in the comparisons section, although the using of the proposed

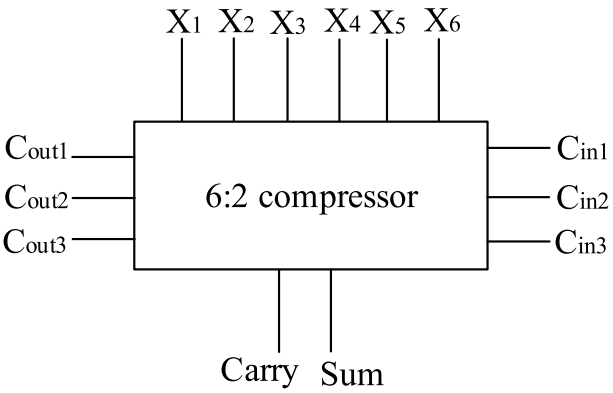
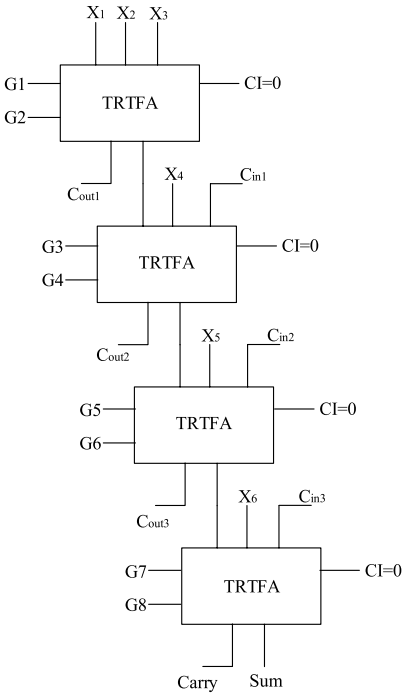


Fig. 25 Circuit representation of 6:2 Compressor



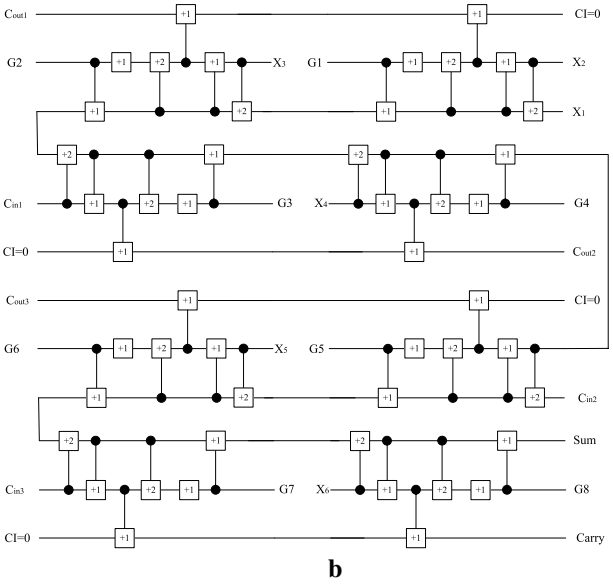


Fig. 26 Quantum reversible ternary 6:2 Compressor using the proposed TRTFA block **a** circuit representation and **b** quantum realization

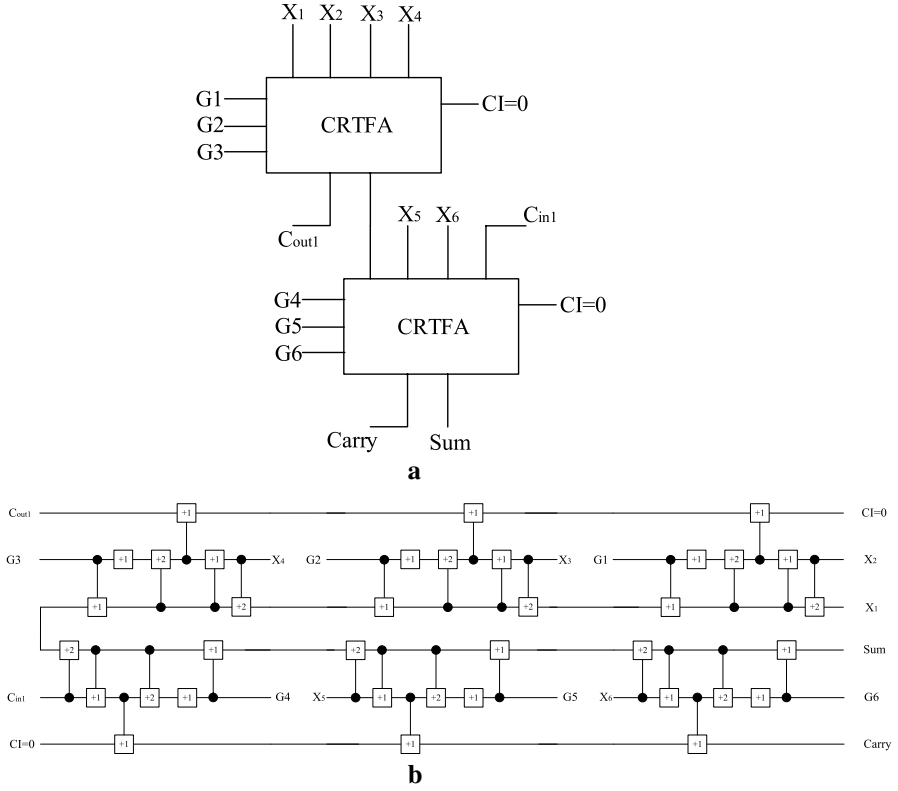


Fig. 27 Quantum reversible ternary 6:2 Compressor using the proposed CRTFA blocks **a** circuit representation and **b** quantum realization

TRTFA block in the 6:2 Compressor design compared to other previous designs has improved performance, but this design is not optimal. As mentioned in the previous section, the reason behind this problem is that not all output capacities are used in the proposed quantum traditional reversible ternary full-adder (TRTFA).

In Fig. 27, a new optimized design of the quantum reversible ternary 6:2 Compressor using the proposed CRTFA circuit has been proposed. As shown in this design, two proposed CRTFA blocks are required. So the quantum cost of this circuit is 36. In addition, this circuit has 2 constant inputs and 6 garbage outputs. Therefore, this circuit will be the most efficient because all output capacities are used in this design.

5 Comparisons and discussions

In this section, we first presents the evaluation of the introduced reversible ternary half-adder circuit with previous designs in [6–8, 12, 32, 33, 37]. Then, we compare the introduced quantum traditional reversible ternary full-adder with all previous

Table 3 Comparison of the introduced quantum reversible ternary half-adder with previous designs

Design in	NOCI	NOGO	QC	HC
[32]	1	1	20	20 γ
[6]	1	1	23	7 ε + 16 γ
[37]	2	2	21	4 ε + 17 γ
[7]	1	1	13	6 ε + 7 γ
[8]	1	1	7	4 ε + 3 γ
[12]	1	1	17	4 ε + 13 γ
[33]	1	1	7	2 ε + 5 γ
Proposed RTHA circuit [17]	1	1	6	6γ

Table 4 Comparison of the introduced traditional reversible ternary full-adder with all previous traditional reversible ternary full-adders

Design in	NOCI	NOGO	QC	HC
[6]	2Explicit + 1Implicit	3Explicit + 1Implicit	50	14 + ε36 γ
[37]	4Explicit + 1Implicit	5Explicit + 1Implicit	42	8ε + 34 γ
[32]	2Explicit	3Explicit	50	50 γ
[38]	1Explicit + 1Implicit	2Explicit + 1Implicit	34	8ε + 26 γ
[8]	1Explicit	2Explicit	14	8ε + 6 γ
[33]	1Explicit	2Explicit	14	4ε + 10 γ
[31]	1Explicit + 2Implicit	2Explicit + 2Implicit	102	22ε + 80 γ
[34]	2Explicit + 2Implicit	3Explicit + 2Implicit	181	Not report
[7]	1Explicit	2Explicit	26	12ε + 14 γ
Proposed TRTFA circuit [17]	1Explicit	2Explicit	12	12 γ

quantum reversible ternary full-adders in [6–8, 31–34, 37, 38]. Finally, a comparison is made between the proposed quantum reversible ternary 6:2 Compressors and quantum reversible ternary 6:2 Compressors designed with previous quantum reversible ternary full-adders.

5.1 Evaluation of the introduced reversible ternary half-adder

Table 3 shows the introduced quantum reversible ternary half-adder circuit analysis with previous designs in terms of number of constant inputs(NOCI), number of garbage outputs(NOGO), delay, hardware complexity(HC) and quantum cost (QC).

As shown in Table 3, the proposed quantum reversible ternary half-adder has the lowest quantum cost compared to all previous designs. Moreover, the number of constant inputs and garbage outputs of the proposed RTHA is equal one.

5.2 Evaluation of the introduced traditional reversible ternary full-adder

Table 4 shows the analysis of the proposed traditional quantum reversible ternary full-adder with previous designs in terms of NOCI, NOGO, delay, HC and QC criteria. As can be seen, the proposed circuit has the lowest quantum cost compared to previous designs. Whereas the proposed TRTFA circuit design uses only sum of 1 or 2 in the base 3 and the number of constant inputs and outputs in this design are 1 and 2, respectively.

As shown in Table 4, the proposed quantum reversible ternary full-adder has the lowest quantum cost compared to all previous designs. Moreover, the proposed TRTFA circuit is superior to other previous designs in [6–8, 31–34, 37, 38] in terms of criteria NOCI and NOGO.

5.3 Evaluation of the proposed reversible ternary 6:2 Compressors

To illustrate the performance of the proposed quantum reversible ternary 6:2 Compressors, quantum reversible ternary versions of the 6:2 Compressor proposed in Fig. 25 are designed using the previous quantum reversible ternary full-adders. The evaluation results are provided in Table 5.

Table 5 Comparison of quantum reversible ternary 6:2 Compressors

Quantum reversible ternary 6:2 Compressor using	NOCI	NOGO	QC	HC
[6]	8 Explicit + 4 Implicit	12 Explicit + 4 Implicit	200	$56\varepsilon + 144\gamma$
[37]	16 Explicit + 4 Implicit	20 Explicit + 4 Implicit	168	$32\varepsilon + 136\gamma$
[32]	8 Explicit	12 Explicit	200	200γ
[38]	4 Explicit + 4 Implicit	8 Explicit + 4 Implicit	136	$32\varepsilon + 104\gamma$
[8]	4 Explicit	8 Explicit	56	$32\varepsilon + 24\gamma$
[33]	4 Explicit	8 Explicit	56	$16\varepsilon + 40\gamma$
[31]	4 Explicit + 8 Implicit	8 Explicit + 8 Implicit	408	$88\varepsilon + 320\gamma$
[34]	8 Explicit + 8 Implicit	12 Explicit + 8 Implicit	724	Not report
[7]	4 Explicit	8 Explicit	104	$48\varepsilon + 56\gamma$
Proposed TRTFA	4 Explicit	8 Explicit	48	48γ
Proposed CRTFA	2 Explicit	6 Explicit	36	36γ

As can be seen in Table 5, the proposed quantum reversible ternary 6:2 Compressors show a 14% and 35% improvement, respectively, in terms of quantum cost, compared to the best previous design in [8, 33]. In addition, the proposed 6:2 Compressor based on the CRTFA circuit has the least constant inputs and garbage outputs.

6 Conclusion

In this paper, we first introduced a new quantum reversible ternary half-adder. In the following, using this quantum reversible ternary half-adder, two efficient reversible versions of traditional and comprehensive quantum reversible ternary full-adders were introduced. Finally, to illustrate the efficiency of the proposed quantum reversible ternary full-adders, various quantum reversible ternary versions of the 6:2 Compressor were proposed. Based on the evaluation results presented in Table 5, the proposed 6:2 Compressors have 14% and 35% improvement, in terms of quantum cost, compared to the best previous designs.

As future work, the use of the proposed circuits in multipliers, dividers and subtractors can reduce the latency and complexity of the circuits.

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